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10/664,982	09/17/2003	David Chong Sook Lim	112055-0040P1	4640

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/664,982
Filing Date: September 17, 2003
Appellant(s): LIM ET AL.

Edwin H. Paul
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/29/2008 appealing from the Office action mailed 8/10/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,531,784	SHIM	3-2003
20030178710	KANG	9-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (US 6,531,784) in view of Kang et al. (US 2003/017810 A1).

Regarding claim 1, Shim (e.g. figs. 9 & 5) shows a die containing package comprising: a die 14 defining electrical die contacts 34, the die contacts arranged along a first and an opposite side of the die (i.e. left side from the geometrical center line and right side from the geometrical center line of the chip), a substrate 30 defining first substrate contacts 22, flattened electrical conductive balls 58 attached to the die contacts and making electrical connection thereto, electrical conductive runs 24 on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts 22, wherein the second substrate contacts are located adjacent to the opposite side of the die, electrically conductive wires 28 with first ends making electrical connections to the first substrate contacts, wherein the wires are formed to run substantially parallel to the surface of the die, and wherein the other ends are horizontally attached to the flattened balls.

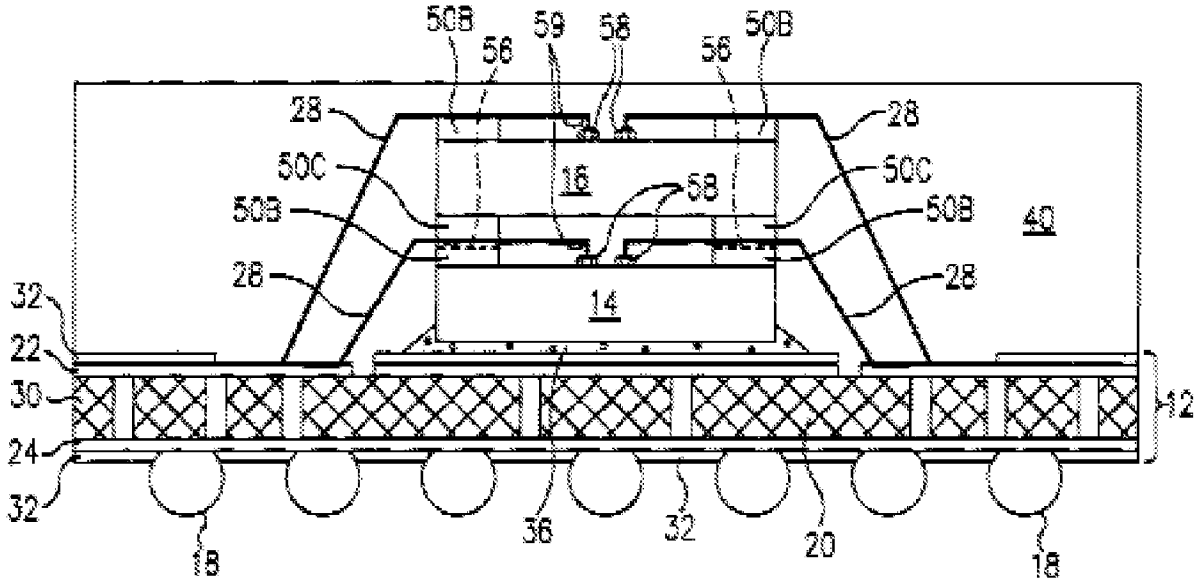
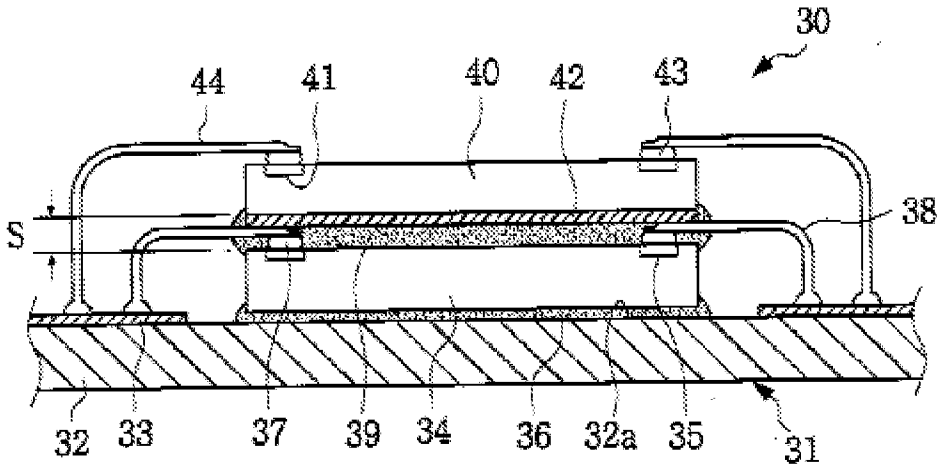


FIG. 9

Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract).



It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

Regarding claim 4, Shim shows that the second substrate contacts are located to accommodate a pin out different from the die.

Regarding claim 5, Shim (e.g. fig. 9) shows process for packaging a die comprising the steps of: defining electrical die contacts, the electrical die contacts arranged along a first and an opposite side of the die (i.e. left side from the geometrical center line and right side from the geometrical center line of the chip), defining a substrate 12 with first substrate contacts 22, flattening an electrical conductive balls 58, attaching the flattened electrically conductive balls to the die contacts, forming electrical conductive runs 22/24 on the substrate 12 that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located

adjacent to the first side of the die, to second substrate contacts 22 wherein the second substrate contacts are located adjacent to the opposite side of the die, connecting electrically conductive wires 28 to the first substrate contacts, running the electrically conductive wires substantially parallel to the surface of the die contacts and attaching the other ends of the wires to the flattened electrically conductive balls thereby making electrical connections therebetween and wherein the other ends remain substantially parallel to the surface of the die. Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

Regarding claim 8, Shim shows that the second substrate contacts are located to accommodate a pin out 18 different from the die.

(10) Response to Argument

Appellant argues that Shim does disclose or suggest runs on layers 22 and 24 that under the die from side to side. Nonetheless, Shim (e.g. fig. 9) shows electrical conductive runs 24 on the substrate 30 that run substantially under the die 14

connecting the first and second substrate contacts 22. Note that the contacts 22 are connected by vias or plated holes. Arguments of counsel cannot take the place of factually supported objective evidence. See, e.g., In re Huang, 100 F.3d 135,139-40, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984).

In response to Appellant argument that the layer 22 and 24 are not runs, it is respectfully noted that conductive layer 22 and 24 function as runs (connection layers), therefore one of ordinary skills in the art would recognized them as runs. Furthermore, Shim shows in an alternative embodiment (e.g. fig. 1) that the conductive layers were patterned as runs.

In response to Appellant Affidavit that that "runner under the die provides the advantage of allowing a die- up die to be packaged in a die-down package. It provides the side to side reversal of the contacts so that the die contacts match those of the package regardless of the "die-up" or "die-down" types", the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See Ex parte Obiaya, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Also, the obviousness rejection was based on the fact that Shim does not teach a flattened ball which is it suggested by Kang. As stated above the use of runs under the die were fully disclosed by Shim.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Leonardo Andújar/

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/David S Blum/

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